Digital Circuits Theory - Laboratory						
Academic year	Laboratory exercises on	Mode of studies	Field of studies	Supervisor	Group	Section
2024/2025	Wednesday 11:45 – 13:15	SSI	Informatics	US	1	1

Report from Exercise No 9 and 10

Performed on: 11.12.2024

Exercise Topic: Registers and Counters

Performed by:

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Task 1

Obtain a 4-bit self-setting ring register counter with the effect of “circling 1”.

Solution

We implemented a 4-bit ring counter circuit. This design ensures continuous circulation of the ”1”.

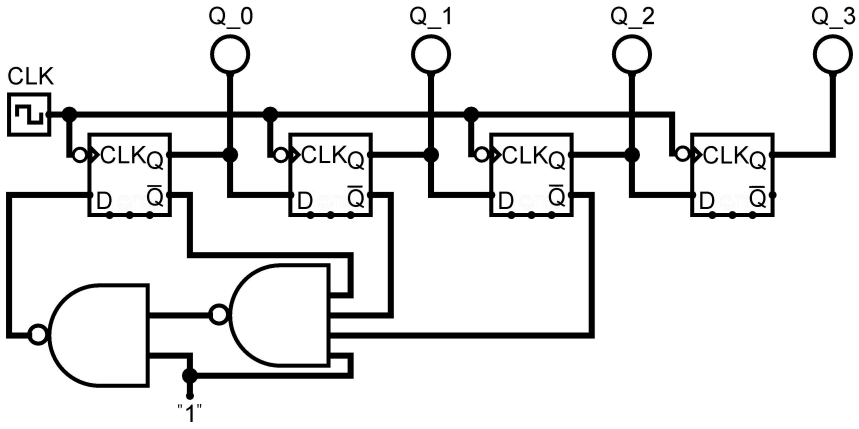

Figure 1 - The circuit diagram for Task 1.

Next we tested our design. From the behavior of the circuit we read a timing chart where a single ”1” circulates through the outputs Q_0, Q_1, Q_2, Q_3.

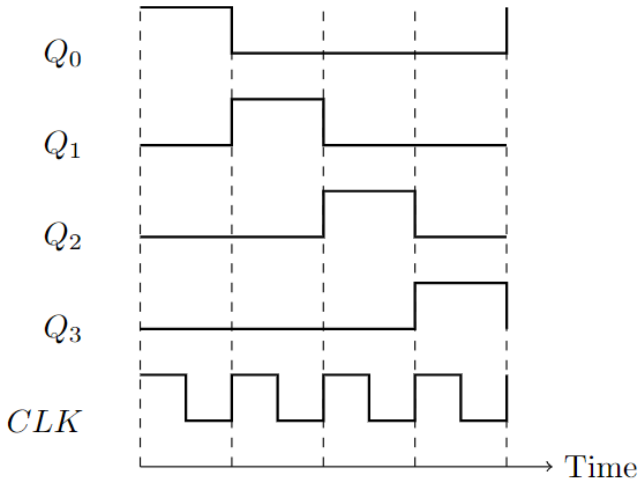

Figure 2 - The timing chart for Task 1.

The register implemented with D type flip-flops, with the feedback loop using NAND gates ensures the effect of circulating ”1” and also provides the self correcting mechanism in case no ”1” or too much ”$1's$” are in the circuit.

Task 2

Obtain a 3-bit linear register with the feedback function defined as $Q_2 \oplus Q_0$.

Solution

The register was implemented using D type flip-flops, with the feedback loop using NAND gates behaving like XOR gate.

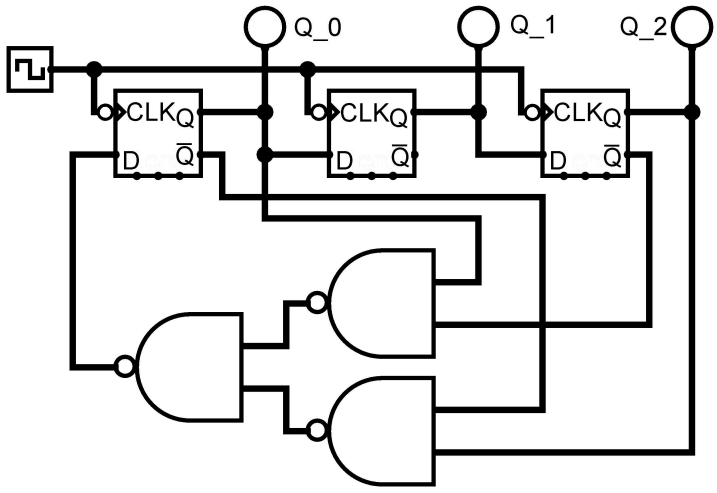

Figure 3 - The circuit diagram for Task 2.

By observing the behavior of the built circuit we created timing chart. The state we did not consider a state where all flip-flops were set to $"0"$, which is illegal state for this particular case.

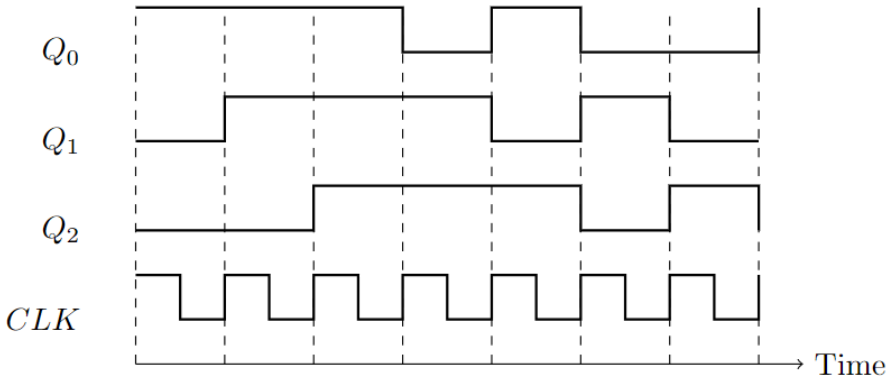

Figure 4 - The timing chart for Task 2.

Issues during laboratory

During implementation we encountered the problem with one of the flipflops as one of its input was not working as expected. We detected the malfunctioning component by testing it on a simpler circuit.

Task 3

Obtain a serial Mod 8 adding counter.

Solution

We started by implementing an adding Mod 8 counter circuit, in which D flip-flops were connected in series, because of that connection the clock signal is only applied to Q_0, which then works as the clock for Q_1 and Q_1 for Q_2.

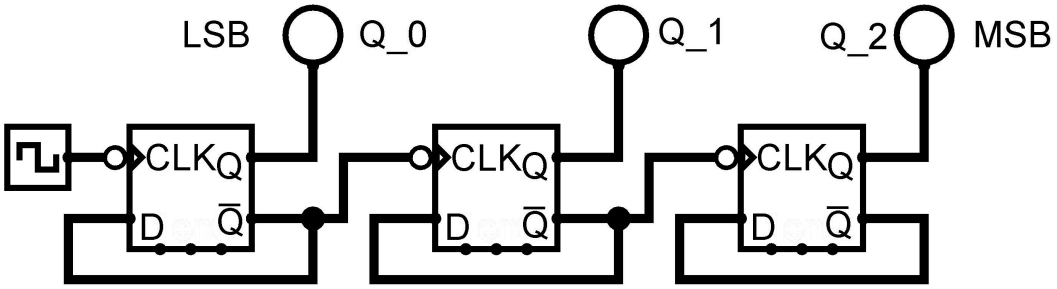

Figure 5 - The circuit diagram for Task 3.

We created a timing chart by observing the circuit, which showed how the counter transitions from one state to another over time. The chart shows how the output increments from 0 to 7 and then cycles back to 0.

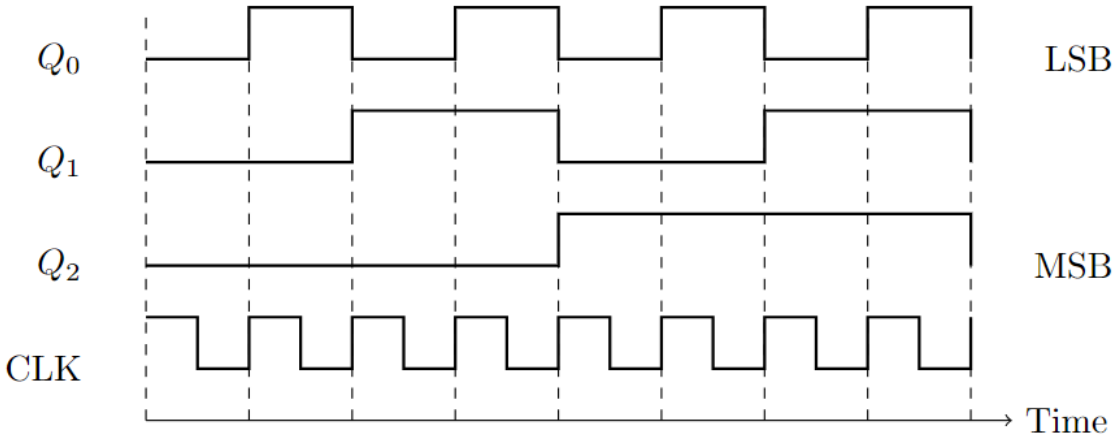

Figure 6 - Timing chart for Mod 8 adding counter.

The timing chart shows how signals (Q_0, Q_1, Q_2) changes over time. Signal Q_0 represents the least significant bit, so it change with each clock pulse, Q_2 represents the most significant bit.

Task 4

Obtain a serial Mod 8 subtracting counter.

Solution

In this task we designed a Mod 8 subtracting counter using D flip-flops. We were able to create a Mod 7 counter circuit that correctly decremented from 7 to 0 and cycled back to 7.

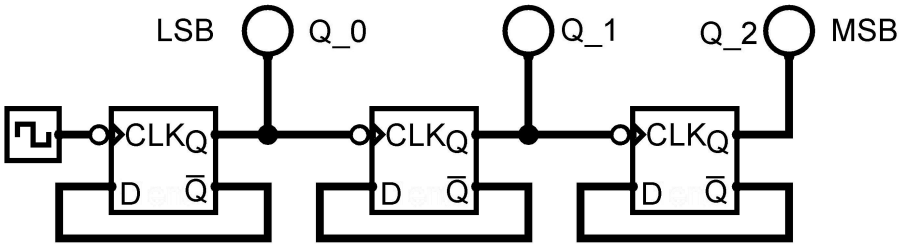

Figure 7 - The circuit diagram for Task 4.

By observing the behavior of the circuit we created a timing chart, that represents the behavior of the subtracting counter. It shows how the counter transitions from one state to another, decrementing from 7 to 0, and then goes back to 7.

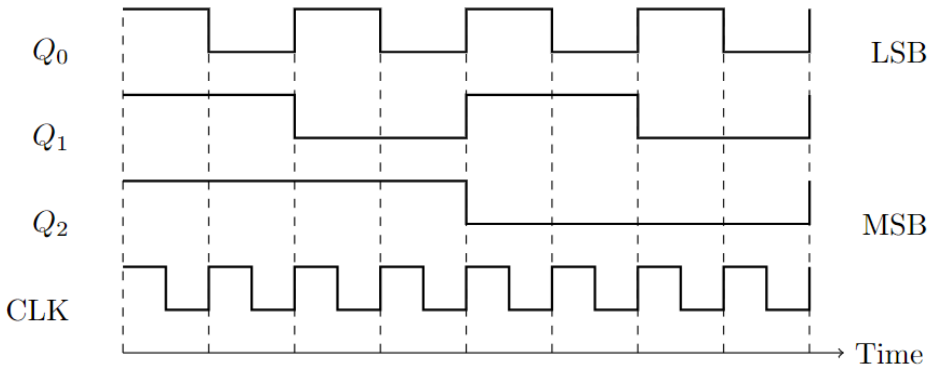

Figure 8 - Timing chart for Mod 8 subtracting counter.

The timing charts presents how signals (Q_0, Q_1, Q_2) changes over time. Signal Q_0 represents the least significant bit, so it changes with each clock pulse, Q_2 represents the most significant bit.

Summary

In these tasks, we were designing and implementing differently working digital circuits focusing on counters and registers using only D type flip-flops. In each task we had to build properly working circuits, analyze their behavior and create timing charts representing how the circuit works over time.