Digital Circuits Theory - Laboratory						
Academic year	Laboratory exercises on	Mode of studies	Field of studies	Supervisor	Group	Section
2024/2025	Wednesday 11:45 – 13:15	SSI	Informatics	KP	1	1

Report from Exercise No 6

Performed on: 15.01.2025

Exercise Topic: Selected arithmetic circuits

Performed by:

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Introduction

The purpose of this exercise was to explore fundamental digital logic components, with a focus on designing and analyzing adders. The tasks involved working with arithmetic combination circuits and testing their functionalities.

Task 1

Obtain full 1-bit adder using NAND gates.

Solution

We started by creating karnaugh maps for C_{i+1} and S_i outputs:

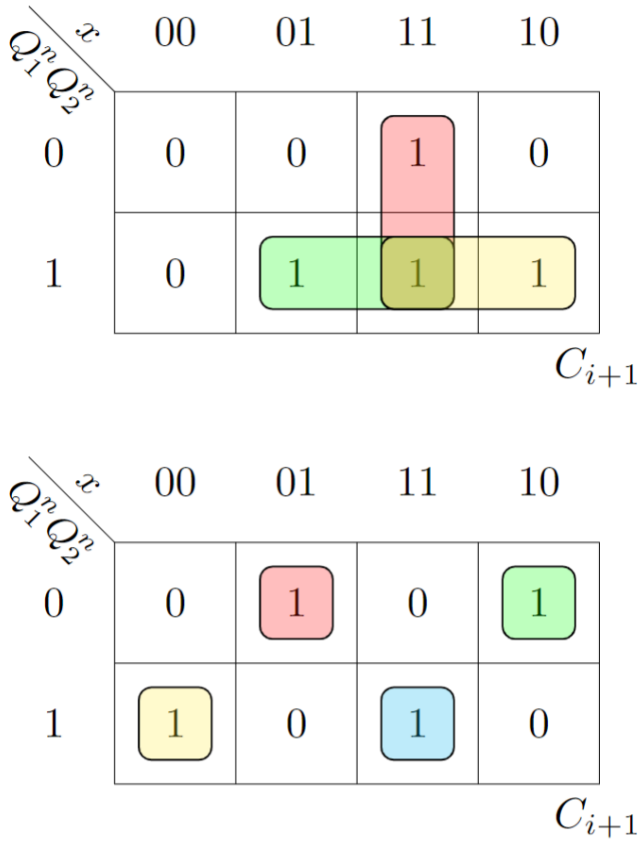

Figure 1 - Karnaugh maps for task 1.

From groups marked on Figure 1 we created logic functions:

$$C_{i+1} = C_i y + x_i y_i + x_i C_i$$

$$S_i = C_i \overline{x_i}\ \overline{y_i} + \overline{C_i}\ \overline{x_i} y_i + C_i x_i y_i + \overline{C_i} x_i \overline{y_i}$$

To obtain solution fitting only NAND gates we transformed the logic functions into:

$$C_{i+1} = \overline{\overline{C_i y} \cdot \overline{x_i y_i} \cdot \overline{x_i C_i}}$$

$$S_i = \overline{\overline{C_i \overline{x_i}\ \overline{y_i}} \cdot \overline{\overline{C_i}\ \overline{x_i} y_i} \cdot \overline{C_i x_i y_i} \cdot \overline{\overline{C_i} x_i \overline{y_i}}}$$

Finally we built the circuit.

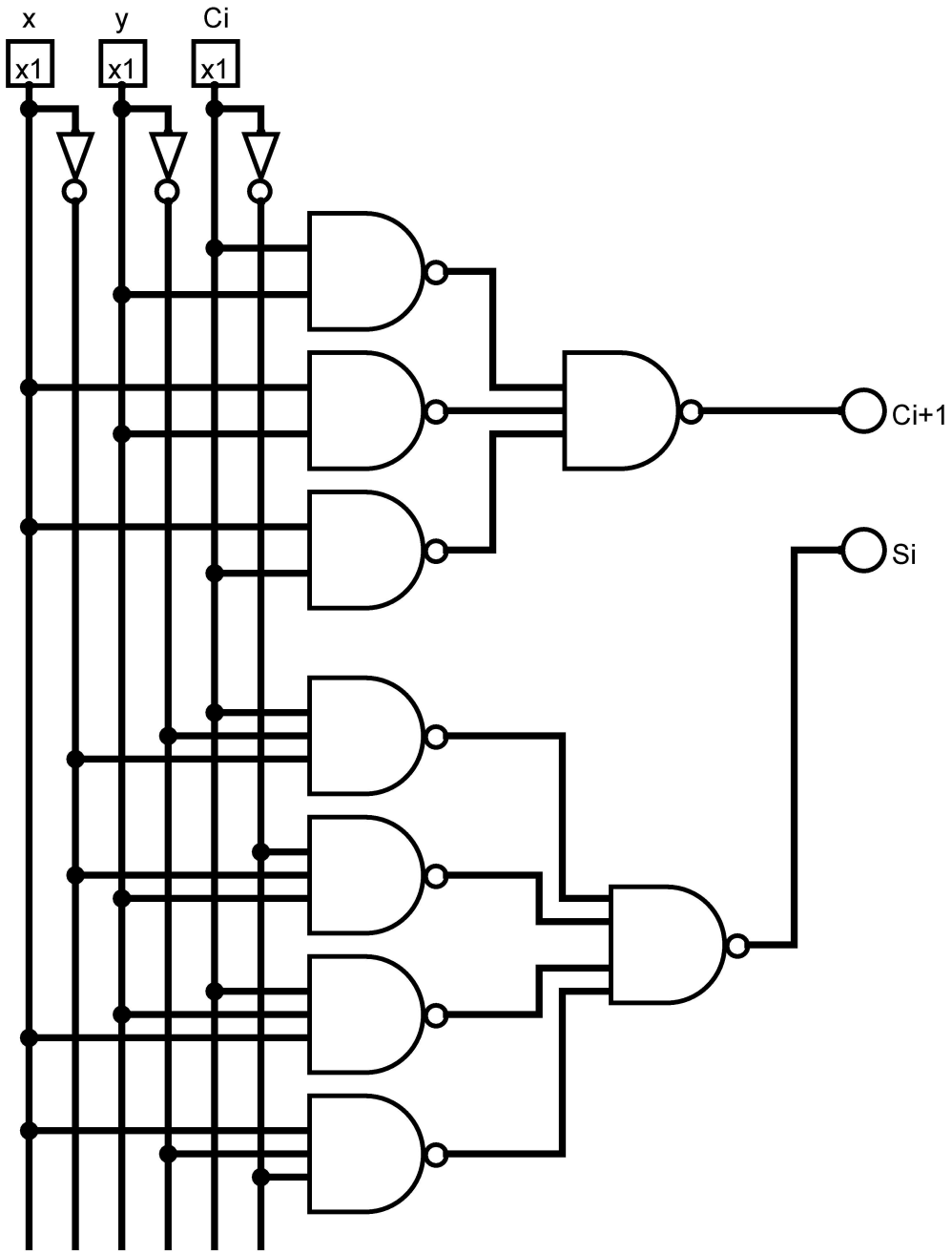

Figure 2 - Diagram for task 1.

Task 2

Using prepared by us test data (pairs of input values and the expected outcomes for the operation), verify the working mode of 4-bit adder with respect to the used representation of binary numbers, whether it adds numbers:

- with sign, in Sign-Magnitude notation
- with sign, in Diminished Radix Complement notation
- with sign, in Radix Complement notation
- without sign

Solution

We prepared such test data:

$$(X)_{10} = 2 \rightarrow (X)_2 = 010$$
$$(Y)_{10} = 4 \rightarrow (Y)_2 = 100$$

We connected the circuit to verify the functionality of the adder

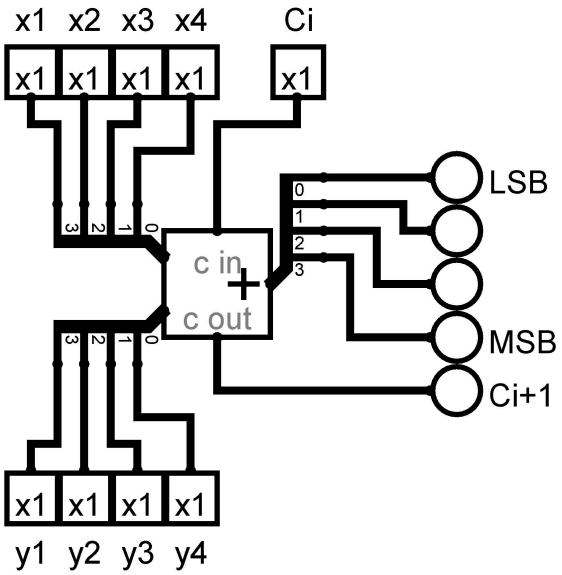

Figure 5 - Connected circuit used to test the adder.

We noticed that the adder was working without sign.

$$0010 + 0100 = 0110 \rightarrow C_{i+1} = 0$$
$$1010 + 0100 = 1110 \rightarrow C_{i+1} = 0$$
$$1010 + 1100 = 0110 \rightarrow C_{i+1} = 1$$
$$0010 + 1100 = 1110 \rightarrow C_{i+1} = 0$$

Task 3

Obtain 5-bit adder from 1-bit adder and 4-bit adder.

Solution

To obtain a properly working circuit we connected the carry (C_{i+1}) form our 1-bit adder to the carry input of the 4-bit adder. The LSB of the 5-bit adder was the Z output from our 1-bit adder. The properly working circuit is shown below:

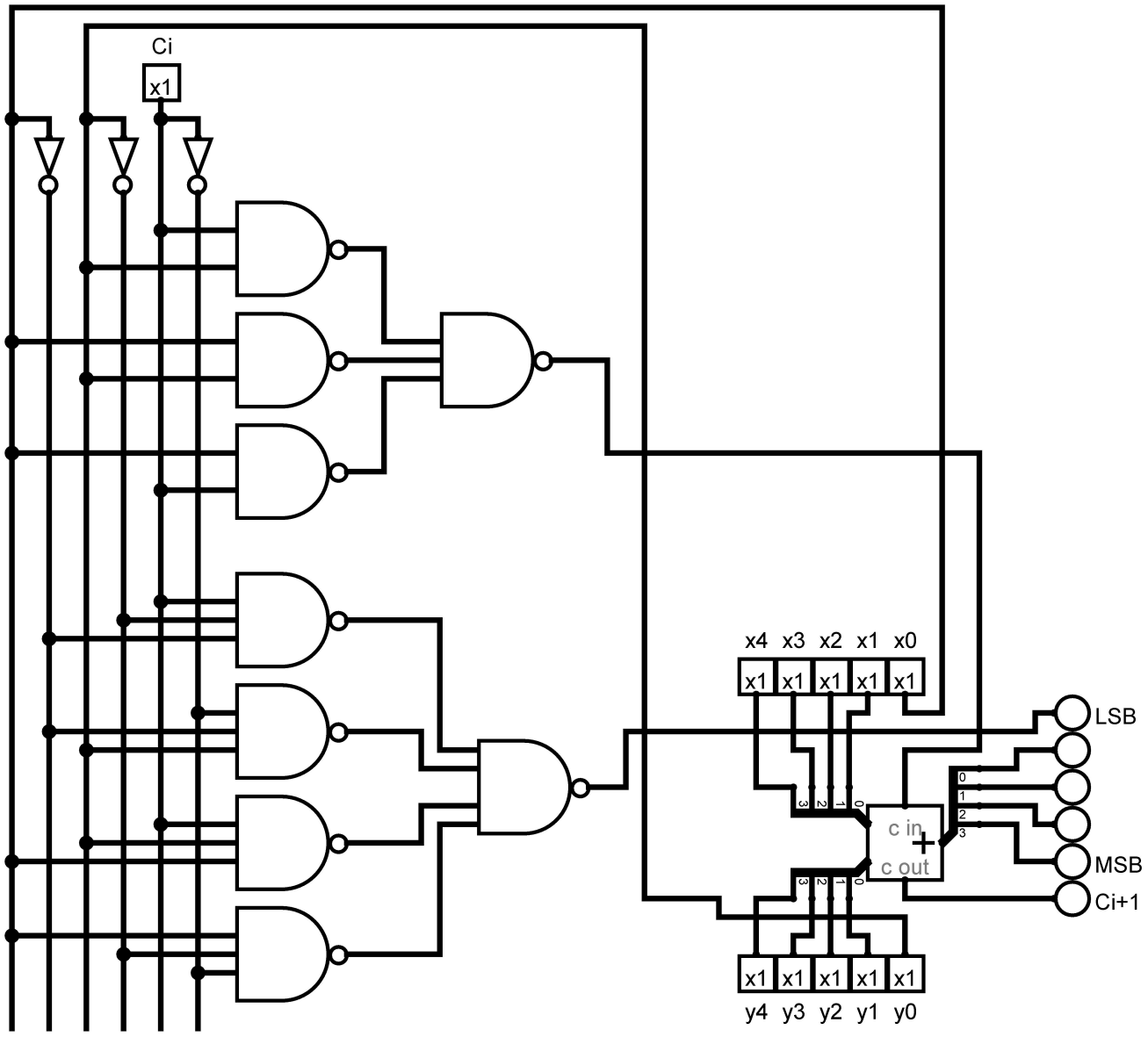

Figure 5 - Diagram for task 3.

Task 4

Modify the circuit from task 3 such to enable switching between RC and DRC notation using button.

Solution

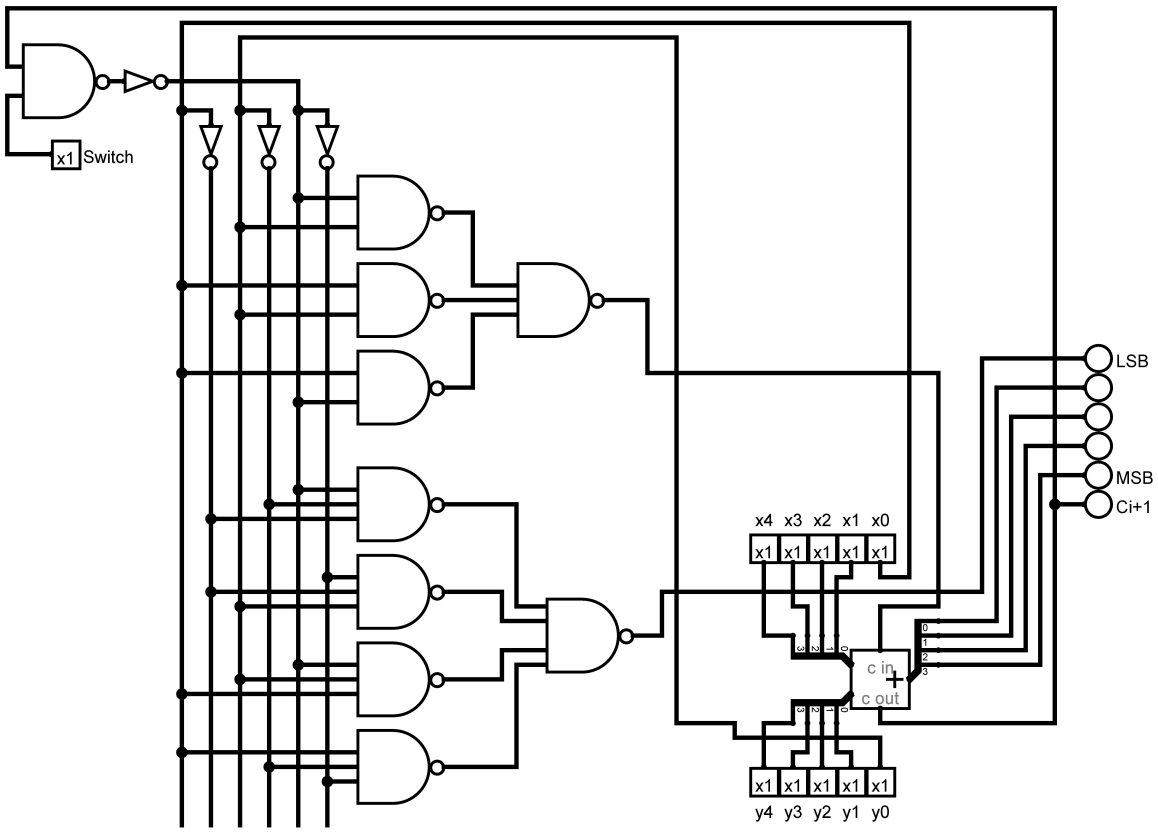

Figure 5 - Diagram for task 4.

As the only difference between notations is last digit we added simple AND gate (negated NAND) acting as carry signal for our 1-bit adder. When the button is on, the circuit acts like a 1's complement (DRC) and when its off it acts as 2's complement (RC).

Summary

During these laboratories, we designed and tested adder circuits. We obtained the working 1-bit adder using NAND gates, verified the behavior of a 4-bit adder with test data, constructed a 5-bit adder by combining both circuits, and modified it for RC and DRC switching. Each task highlights essential principles in digital circuit design.