Digital Circuits Theory - Laboratory						
Academic year	Laboratory exercises on	Mode of studies	Field of studies	Supervisor	Group	Section
2024/2025	Wednesday 11:45 – 13:15	SSI	Informatics	DP	1	1

Report from Exercise No 3

Performed on: 30.10.2024

Exercise Topic: Bistable devices

Performed by:

Piotr Copek
Zuzanna Micorek

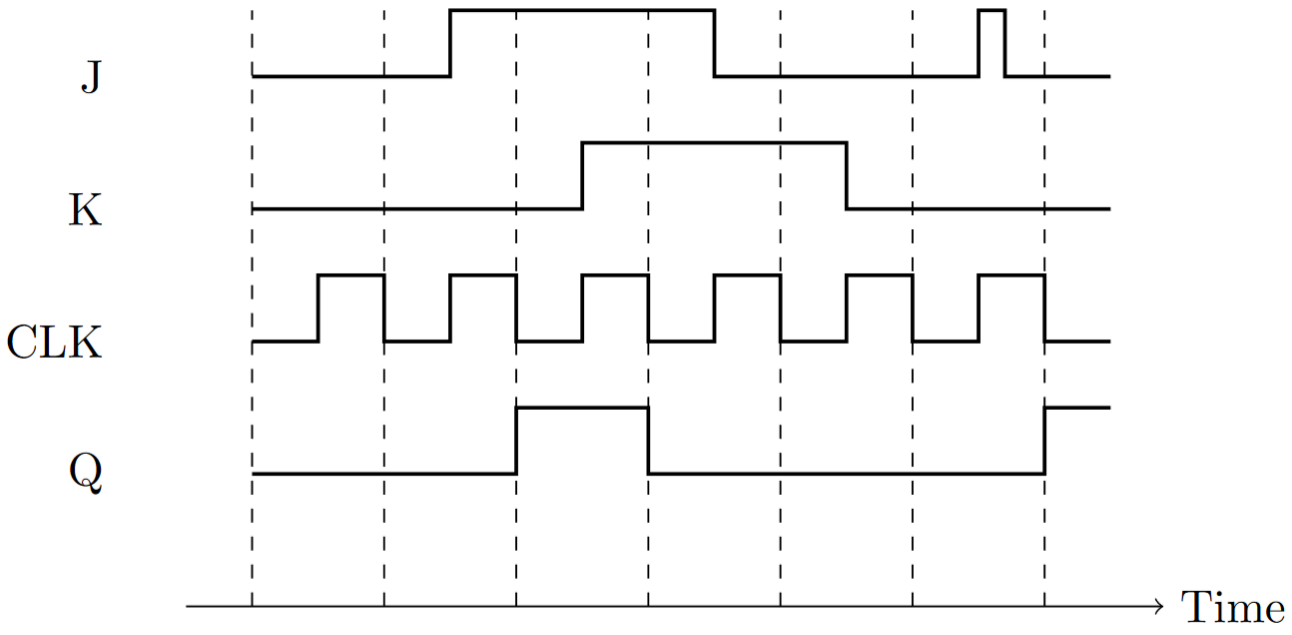
Introduction

In these labs, we explored the fundamental behavior of bistable devices, focusing on JK and D flip-flops and their roles in digital circuits. We examined the triggering mechanisms of both synchronous and asynchronous flip-flops, observing how inputs and clock signals affect their outputs. By using timing charts, we identified the active states and dominance of various inputs, helping us understand potential error conditions and how to manage them in circuit design. This hands-on experience with flip-flops and their triggering types has provided insight into their application in building reliable sequential logic systems.

Task 1

Recognize the triggering way of the synchronous JK flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing charts used to resolve the problem.

Solution



[Figure 1] - Timing chart for exercise 1 executed on JK flip-flop.

To identify the triggering type of the synchronous JK flip-flop, we set up a circuit with a

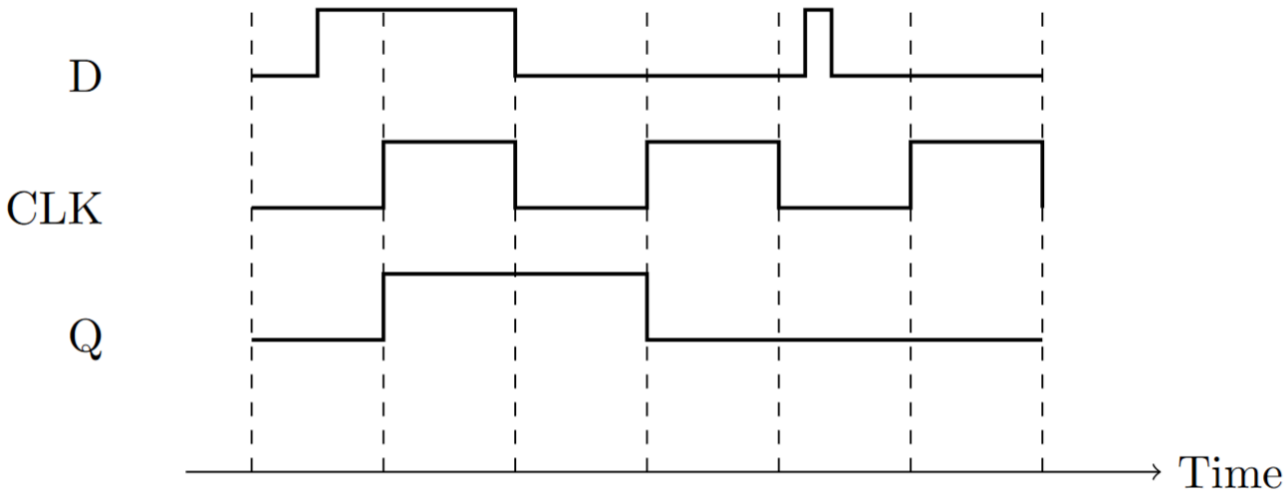
manually controlled clock. We toggled the clock input and observed how the flip-flop responded to changes in the J and K inputs. We noticed that device was triggered by falling edges.

During our testing, we observed "1s catching." This means that if the input signal was briefly set high just before the active clock edge and then turned off, the flip-flop still captured that high signal. This showed us that the flip-flop could catch brief input signals before the clock edge, helping us understand its triggering sensitivity and behavior under different timing conditions.

Task 2

Recognize the triggering way of the synchronous D flip-flops (gated latch, master slave with or without 1s and 0s catching, or positive or negative edge-triggered). Draw timing charts used to resolve the problem.

Solution



[Figure 2] - Timing chart for exercise 2 executed on D flip-flop.

To identify the triggering type of the synchronous D flip-flop, we set up a circuit with a manually controlled clock and observed how the flip-flop responded to changes in the D input.

In this case, we found that the D flip-flop was sensitive to the rising edge of the clock. Unlike the JK flip-flop, there was no "1s catching" observed. The D flip-flop only responded to the

input signal at the precise moment of the rising edge, ignoring any brief signals that appeared before the clock transition. This confirmed that the D flip-flop strictly followed edge-triggered behavior without catching transient input signals.

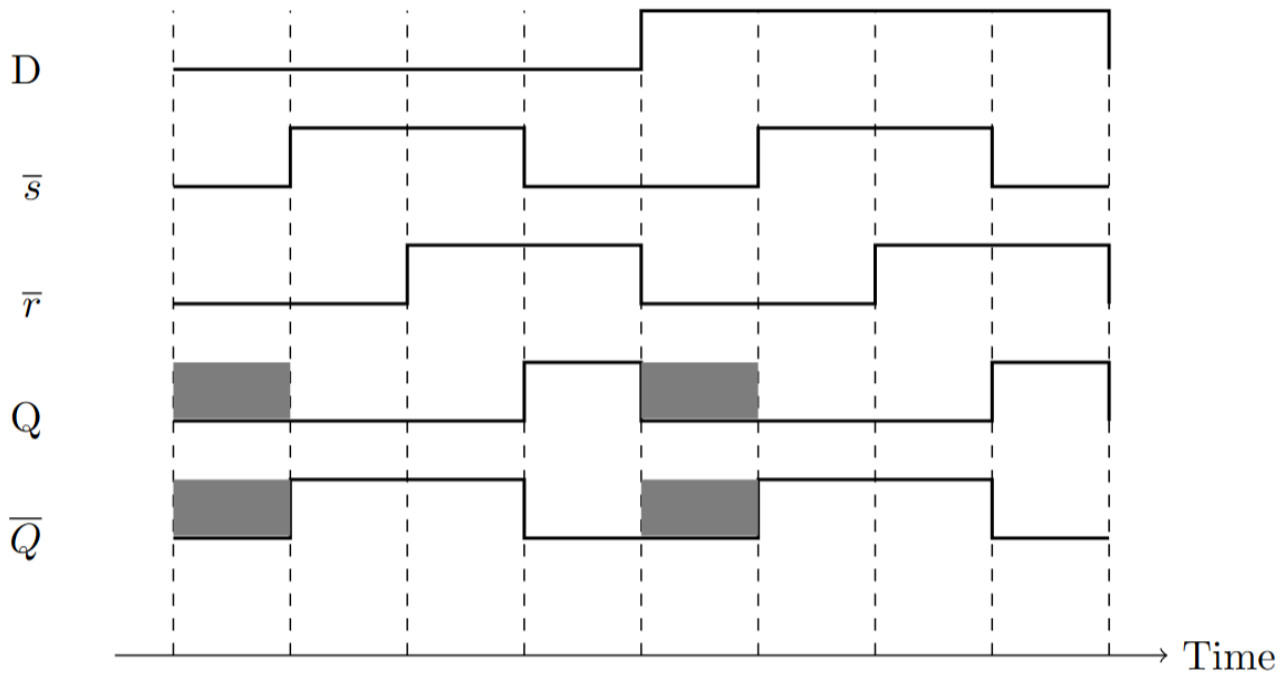
Task 3

Use only asynchronous inputs of the synchronous D flip-flop to determine their active value and which of them is dominant. Draw timing charts used to resolve the problem.

Solution

To determine the active values and dominance of the asynchronous inputs of a synchronous D flip-flop, we focused on the $\overline{s}$ and $\overline{r}$ inputs being set to illegal state which is $\overline{s} = 0$ and $\overline{r} = 0$.

When both inputs are low and the D input is either 0 or 1, the output becomes undefined. Therefore, no input is dominant in this scenario.



[Figure 3] - Timing chart for exercise 3 executed on asynchronous D flip-flop. Grayed out area represents illegal state of flip-flop.

D	¬s	¬r	Q	¬Q
0	0	0	ILLEGAL	
0	1	0	0	1
0	1	1	0	1
0	0	1	1	0
1	0	0	ILLEGAL	
1	1	0	0	1
1	1	1	0	1
1	0	1	1	0

[Figure 4] - Truth table for exercise 3 executed on asynchronous D flip-flop.

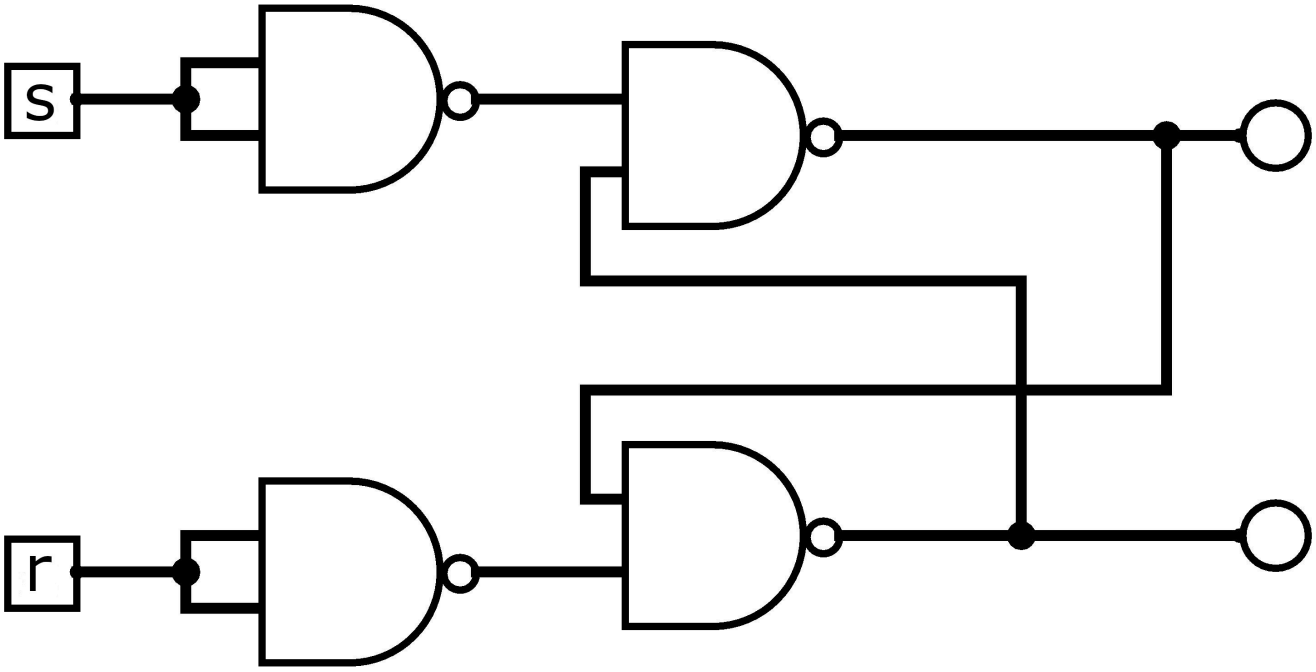
Task 4

Observing race effect in sr flip-flop built from NAND and $\overline{s}\,\overline{r}$ flip-flop built from NOR gates.

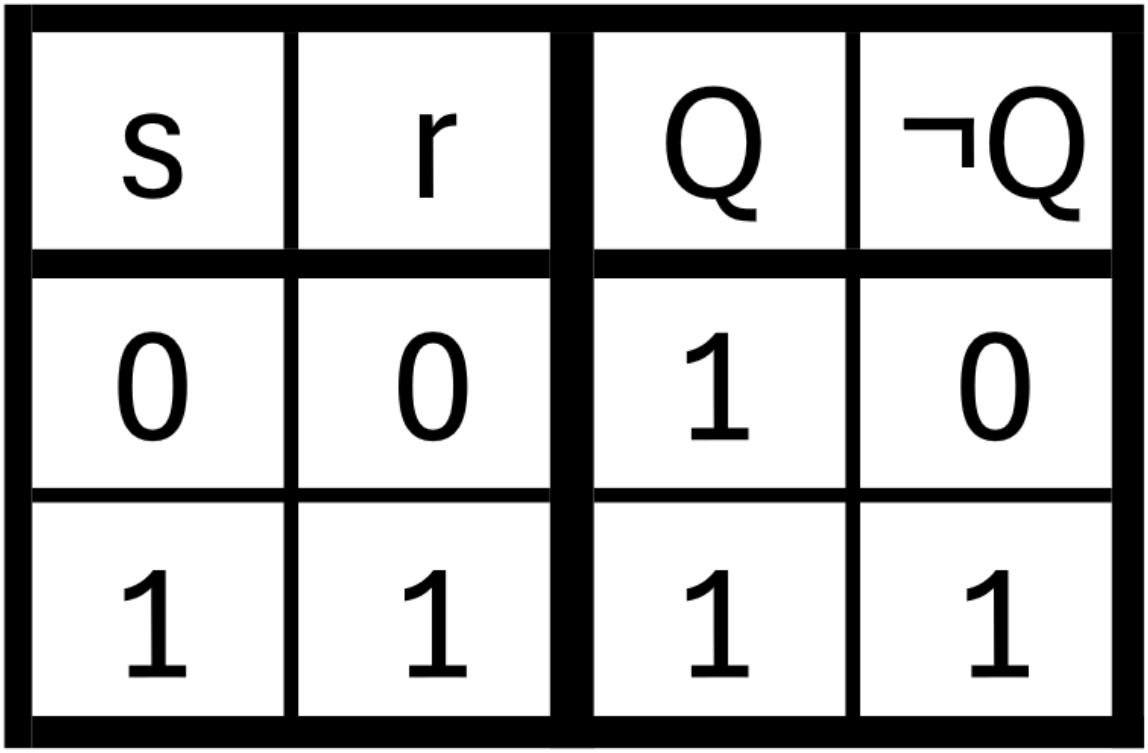
Solution

NAND

We began by constructing an sr flip-flop using NAND gates. Following this, we examined the output for specific input combinations as indicated in the truth table (Figure 6). The outputs matched our expectations with this particular configuration utilizing TTL technology.



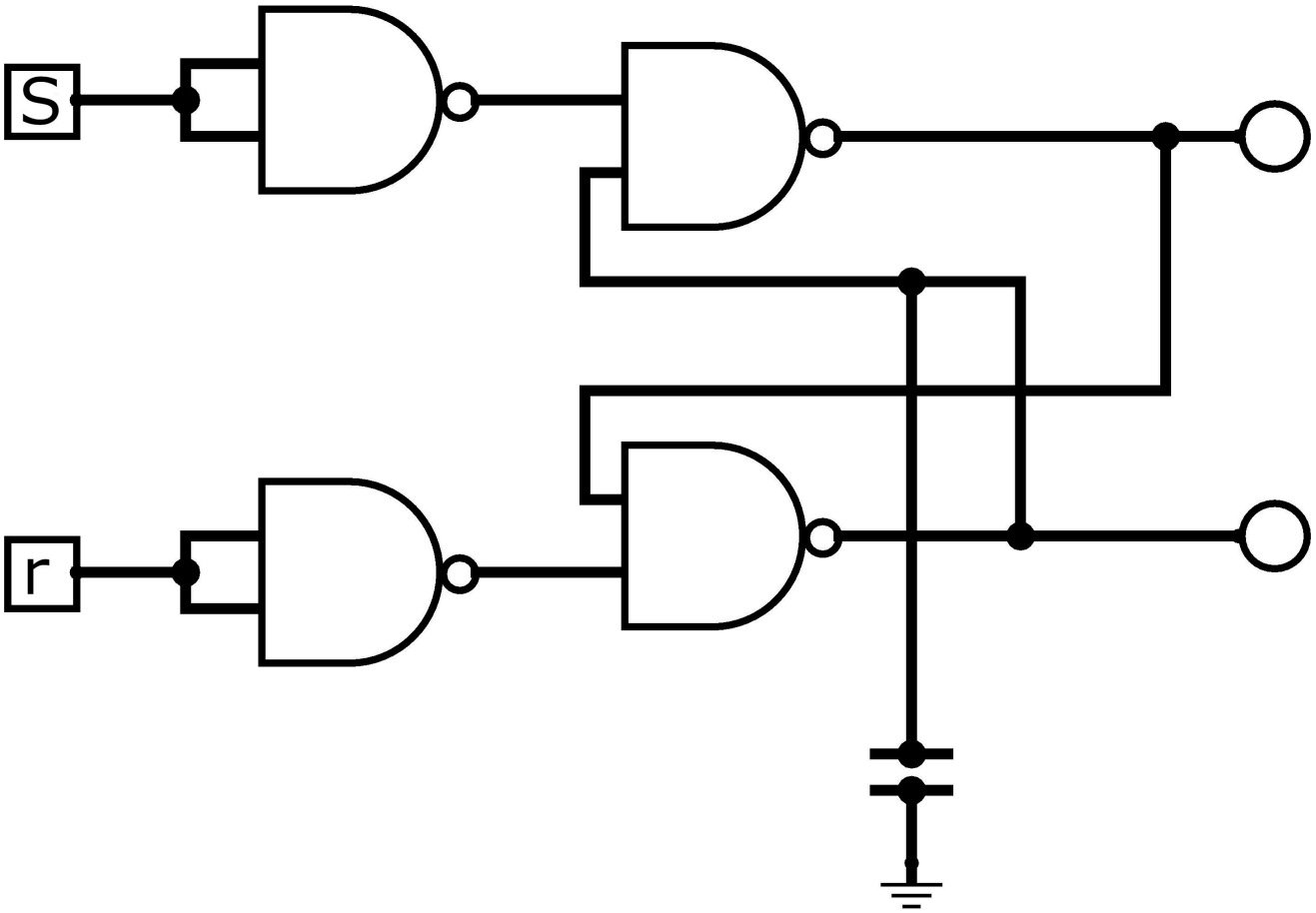
[Figure 5] - sr flip-flop built from NAND gates.



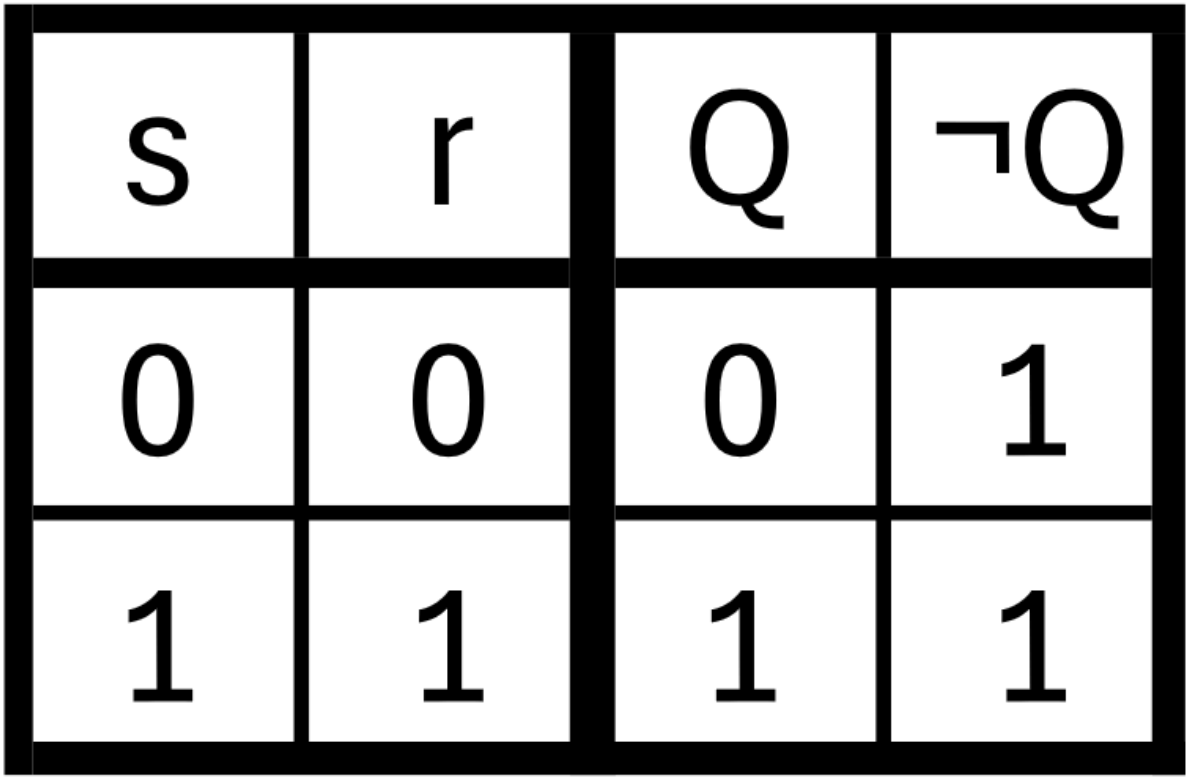
s	r	Q	¬Q
0	0	1	0
1	1	1	1

[Figure 6] - Truth table for sr flip-flop built from NAND gates (Figure 5).

Next, we replaced the short cables connecting the feedback loops and briefly touched one of them as illustrated in the schematic diagram (Figure 7). This manipulation caused the outputs to reverse in the $s = 0$ and $r = 0$ combination, in contrast to the flip-flop where the cable was not held.


S
r

[Figure 7] - sr flip-flop built from NAND gates with small capacitor connected to ground.



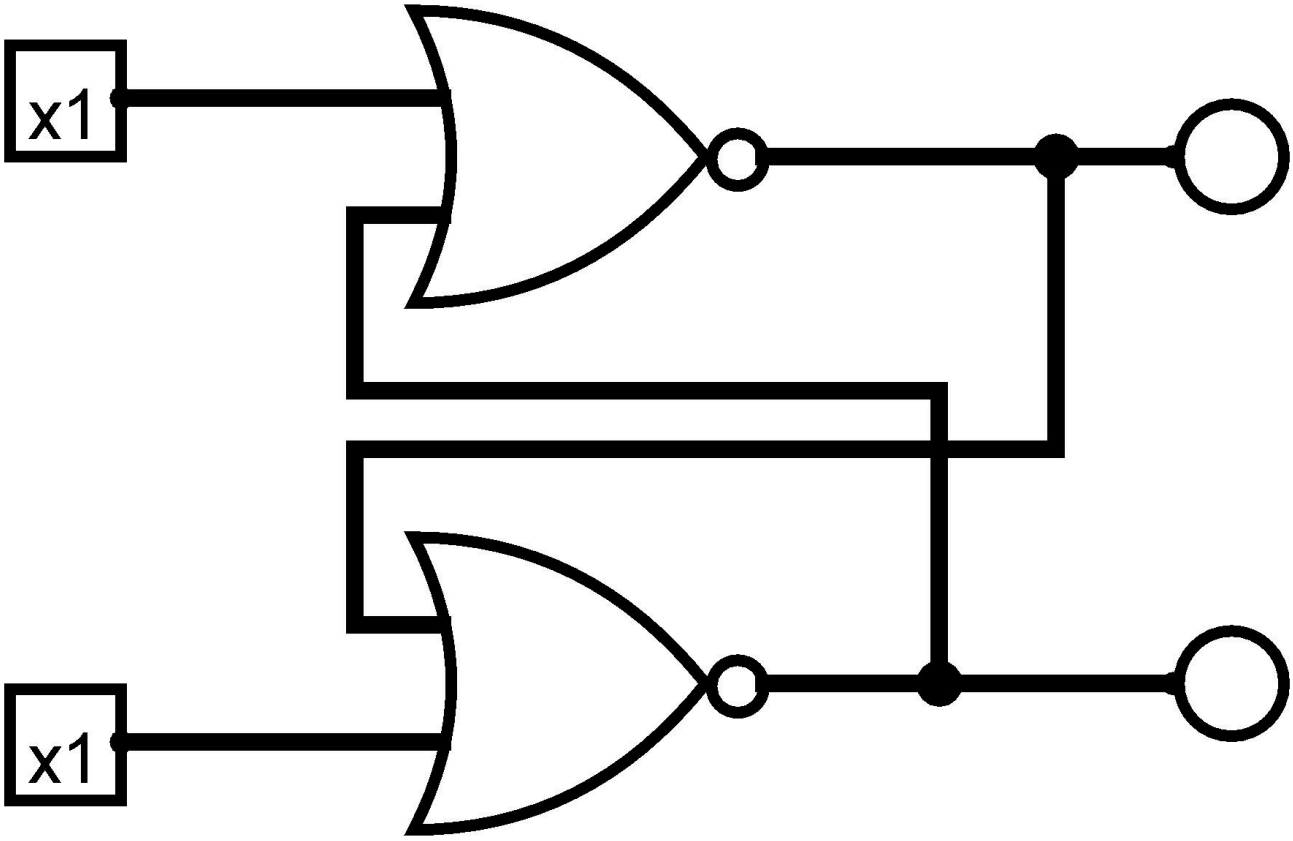
s	r	Q	¬Q
0	0	0	1
1	1	1	1

[Figure 8] - Truth table for sr flip-flop built from NAND gates (Figure 7).

Through this experiment, we observed the race effect in the SR flip-flop built from NAND gates. The manipulation of the feedback loop demonstrated how slight changes in the circuit could lead to unexpected output states. This highlights the sensitivity of flip-flops to their feedback configurations and emphasizes the importance of stable connections in digital circuits.

NOR

We began by constructing an $\overline{s}\,\overline{r}$ flip-flop using NOR gates. Following this, we examined the output for specific input combinations as indicated in the truth table (Figure 10). The outputs matched our expectations with this particular configuration utilizing TTL technology.



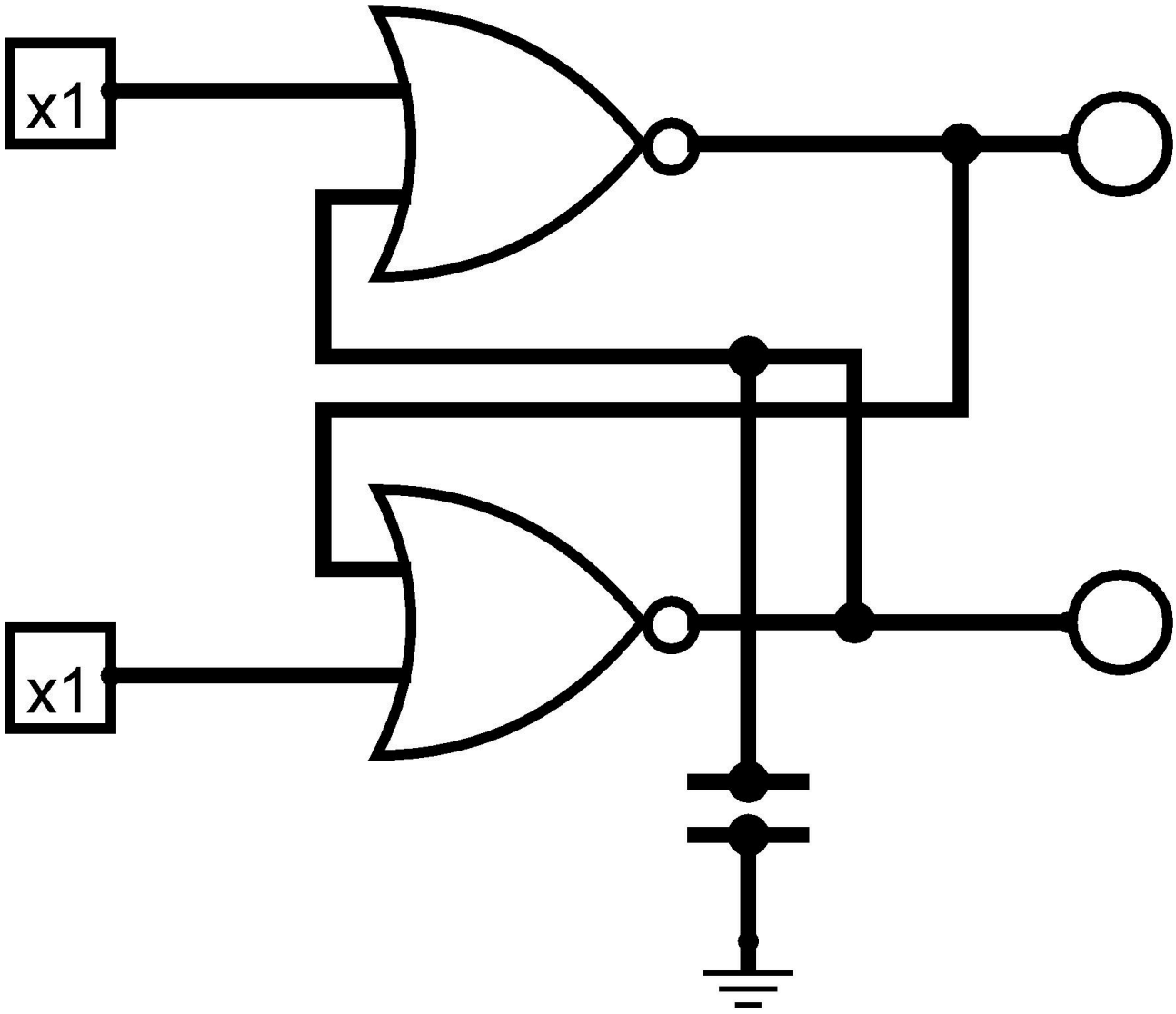
[Figure 9] - $\overline{s}\,\overline{r}$ flip-flop built from NOR gates.

¬S	¬r	Q	¬Q
0	0	1	0
1	1	ILLEGAL	

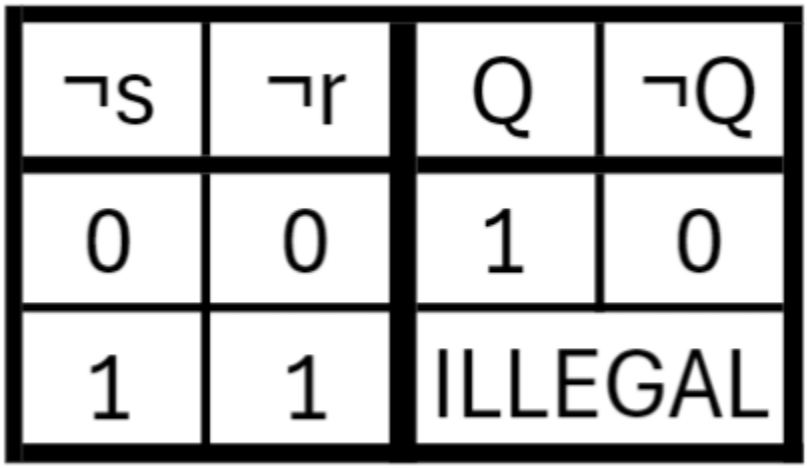
[Figure 10] - Truth table for $\overline{s}\,\overline{r}$ flip-flop built from NOR gates (Figure 5).

Next, we replaced the short cables connecting the feedback loops and touched one of them as illustrated in the schematic diagram (Figure 11). This manipulation did not cause the outputs to reverse in the $s = 0$ and $r = 0$ combination, in contrast to the sr flip-flop built from NAND

gates.



[Figure 11] - sr flip-flop built from NOR gates with small capacitor connected to ground.



¬S	¬r	Q	¬Q
0	0	1	0
1	1	ILLEGAL	

[Figure 12] - Truth table for $\overline{s}\,\overline{r}$ flip-flop built from NOR gates (Figure 9).

In this experiment, we successfully constructed an $\overline{s}\,\overline{r}$ flip-flop using NOR gates and verified its functionality against the expected output as per the truth table. Unlike the sr flip-flop built from NAND gates, the manipulation of the feedback loop in the NOR gate configuration did not lead to any reversal of outputs when both inputs were low. This indicates that the NOR flip-flop is more stable under similar conditions compared to its NAND counterpart.

Final conclusions and observations

In these labs, we explored the behavior of bistable devices, focusing on JK and D flip-flops, as well as SR flip-flops built from NAND and NOR gates. The main point we learned during this laboratories:

- We found that the JK flip-flop in TTL technology is triggered by falling edges and can catch brief high signals "1s catching", while the D flip-flop only responds to rising edges without capturing transient signals.
- When testing the asynchronous inputs of the D flip-flop, we discovered that with both Set and Reset inputs low, the output becomes undefined regardless of the D input. This highlights the need to manage inputs carefully to avoid unstable (illegal) outputs.

- Our experiments with NAND and NOR sr flip-flops demonstrated how changes in feedback loops can affect output stability. The NAND flip-flop was sensitive to changes, leading to unexpected outputs, while the NOR flip-flop was more stable in the same conditions. This indicates the importance of feedback design in flip-flop circuits.
- Overall, understanding flip-flop behavior is crucial for creating reliable digital circuits. Factors like triggering type, feedback stability, and input handling are key to preventing errors.

These labs helped us grasp how flip-flops work and their challenges, which will be valuable in future digital electronics projects.