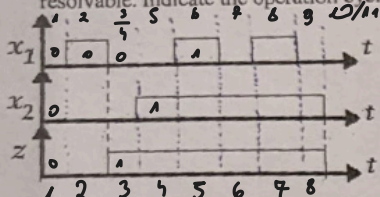


1.1. Based on the time diagram below complete the related SST. Insert correct boundaries to make the table resolvable. Indicate the operation cycle of the control circuit. (1.5 pt).



Phase	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
1	2 ⁰	x ₁	-	+	-		+	-	+	-		-	+	-		+	-	+	-		
2	2 ¹	x ₂	-		+					-		-			+					-	
3	2 ²	z	-	←	+	→				-	←	+	→								-
NCS	0 ₀	1 ₀	0 ₁	4 ₁	6 ₁	7 ₁	6 ₁	7 ₁	6 ₁	7 ₀	0 ₀	1 ₀	9 ₀	8 ₀	12 ₀	14 ₀	6 ₀	7 ₀	6 ₀	7 ₀	4 ₀

test of boundaries || seems okay

1.2. For the SST as below with boundaries inserted as needed provide a resolvable SST and indicate the operation cycle of the circuit (1 pt).

Phase	1	2	3	4	5	6	7	8	9	10	11	12	1
2 ⁰	a	+					-	+		-		+	
2 ¹	b	+	-		+	-	+				-		+
2 ²	x	-	←	+	→				-				
NCS	3 ₀	1 ₁	5 ₁	7 ₁	5 ₁	7 ₁	6 ₁	7 ₀	3 ₀	2 ₀	0 ₀	1 ₀	3 ₀

$\overline{I}$ and $\overline{II}$ +
 $\overline{II}$ and $\overline{IV}$ -

Phase	1	2	3	4	5	6	7	8	9	10	11	12	1
2 ⁰	a	+					-	+		-		+	
2 ¹	b	+	-		+	-	+				-		+
2 ²	x	-	←	+	→				-				
2 ³	q	←	+	→			-	←	+	→		-	
NCS	3	11	9	13	15	13	15	14	6	7	3	11	10

we don't really care

nah

1.3. For the Boolean function of four input variables and one output defined as below provide Boolean expressions for input functions of a sr flip-flop (please remember to fill the Karnaugh maps beforehand) (2,5 pkt).

$$Z = \sum (2,6,9,12,13,14)_{qzba}$$

$$Z = \prod (0,1,3,4,8,10,11,15)_{qzba}$$

$$\overline{s} = \overline{q} + \overline{b} + a$$

$$\overline{r} = \overline{q} + b$$

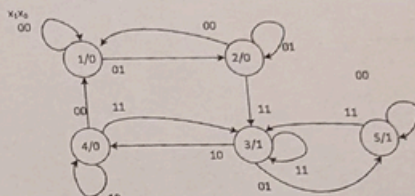
qz	ba	00	01	11	10
00		0	0	0	1
01		0	-	-	1
11		1	1	0	1
10		0	1	0	0

qz	ba	00	01	11	10
00					
01					
11					
10					

$$s = qb\overline{a} \quad \overline{s} = \overline{qb\overline{a}} = \overline{q} + \overline{b} + a$$

$$r = q\overline{b} \quad \overline{r} = \overline{q} + b$$

2.1 For an asynchronous sequential circuit defined by the graph below provide a primary transition table for the control routine. (1 pt).



ab	00	01	11	10	XY
1	2				0
1	2	3			0
1	5	3	4		1
1	3	3	3		0
1	3	3			1

2.1. For the primitive flow map of a control routine as below carry out reduction of equivalent and [pseudo-equivalent states (1st step of minimization) (1.5pt).

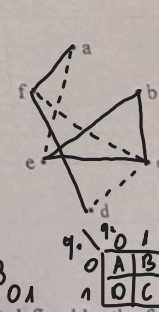
ab	00	01	11	10	W
1	1	8		2	0
2	3		5	2	1
3	3				1
4			5	4	0
5	1	6	5		0
6	4	6			0
7	2	8			0
8	9	8			1
9	9	8		10	1
10	1			10	0

States to be merged:
1-4
2-4 → 2-3
3-9
5-6-10

ab	00	01	11	10	W
1,7	1	8		2	0
2,3,4	3		5	3	1
5,6,10	1	6	5	10	0
9	9	8			1

2.2. For the flow map of a control circuit as below, carry out reduction of compliant states (2nd step of minimization). Draw a graph for reduction of states. Then provide a non-encoded reduced transition table for internal states of a Moore model of a Finite State Machine as well as an encoded table for internal state. Eliminate a possible race effect, if any. (1.5pt).

x ₁ x ₂	00	01	11	10	W
a		2	1	4	0
b	5	2	3		1
c		2	3	4	1
d	6		3	4	0
e	5	2		4	1
f	6	2		4	0



(A) a, d
(B) d
(C) b, c, e

x ₁ x ₂	00	01	11	10
A	6	2	1	4
B	5	2	3	4
C	6		3	4
D	6			

x ₁ x ₂	00	01	11	10
A 00	00	01	00	01
B 01	01	01	01	11
C 11	10		01	11
D 10	00			

2.3. Analyze a control circuit defined by the following flow map in terms of possible races - encircle states and specify a race type for the specific map (1 pt).

x ₁ x ₂	00	01	11	10
q ₁ q ₂	00	01	01	00
00	00	01	01	00
01	00	01	01	10
11	00	01	10	11
10	10	01	10	10

critical race

critical race

noncritical race