Task 3 (US)
Design a parallel [redacted] Mod 6 counter, counting in Gray code. Ensure asynchronous illegal state recovery. Present a solution in the form of logic expressions given for excitation functions for flip-flops, without drawing a logical diagram. There are available flip-flops of JK, T, and D type, but only one flip-flop for each type can be used.

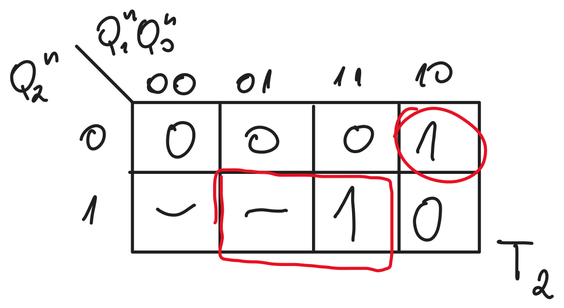
5 - 4 - 3 - 2 - 1 - 0

	W	S^n
0	000	000
1	001	001
2	011	010
3	010	011
4	110	100
5	111	101
6	101	110
7	100	111

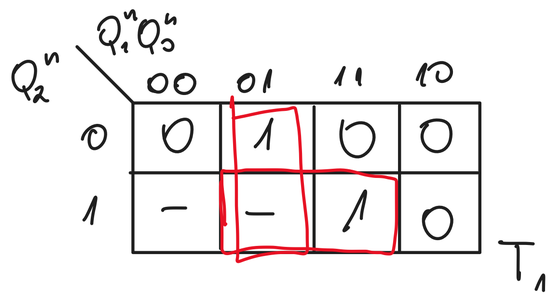
Gray code	Q_2^n	Q_1^n	Q_0^n	Q_2^{n+1}	Q_1^{n+1}	Q_0^{n+1}	T_2^n	T_1^n	T_0^n	$\overline{S}_2$	$\overline{r}_1$	$\overline{S}_1$	$\overline{r}_1$	$\overline{S}_0$	$\overline{r}_0$
0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1
1	0	0	1	0	1	1	0	1	0	1	1	1	1	1	1
3	0	1	0	1	1	0	1	0	0	1	1	1	1	1	1
2	0	1	1	0	1	0	0	0	1	1	1	1	1	1	0
7	1	0	0	0	0	0	-	-	-	1	0	1	-	1	-
6	1	0	1	0	0	0	-	-	-	1	0	1	-	0	1
4	1	1	0	1	1	1	0	0	1	1	1	1	1	1	1
5	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1

D_2^n D_1

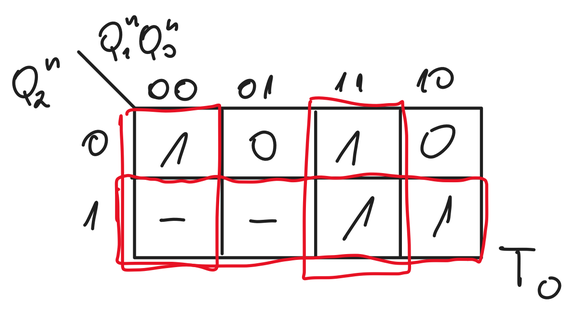
$\overline{S}_2 = \overline{r}_1 = \overline{S}_1 = \overline{r}_0 = 1$



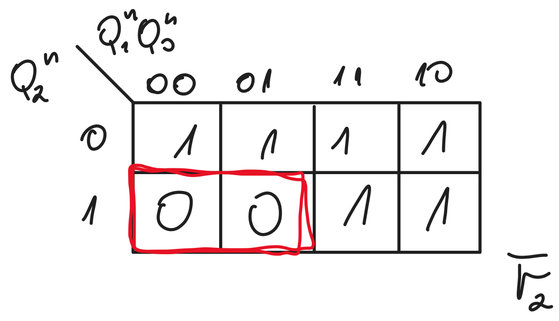
$T_2 = Q_2^n Q_0^n + \overline{Q_2^n} Q_1^n \overline{Q_0^n}$



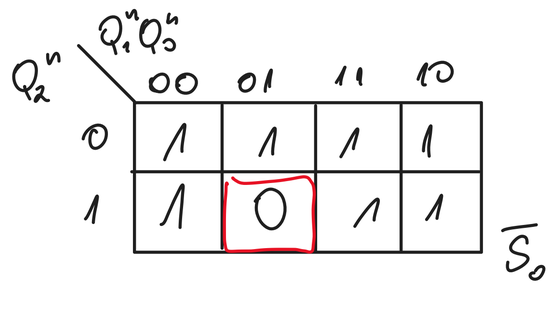
$T_1 = Q_2^n Q_0^n + \overline{Q_1^n} Q_0^n$



$T_0 = Q_2^n + \overline{Q_1^n}\,\overline{Q_0^n} + Q_1^n Q_0^n$



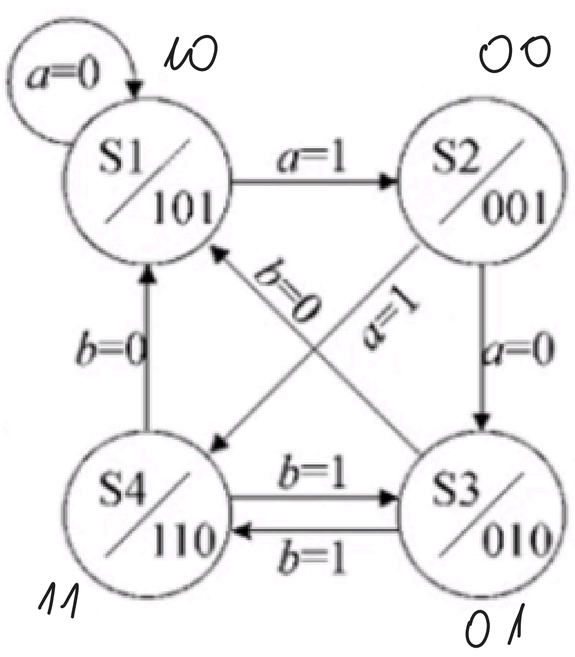
$\overline{r}_0 = \left(\overline{Q_2^n} + Q_1^n\right)$



$\overline{S}_0 = \left(\overline{Q_2^n} + Q_1^n + \overline{Q_0^n}\right)$

Task 4 (BZ)
Design microprogrammable circuit with 3 outputs (Y_2, Y_1, Y_0) and 2 inputs (a, b), with the working cycle described with the presented state diagram. Provide the solution in the form of a logical diagram of the selected microprogrammable structure and corresponding memory content table.

NOTE: the grade depends on solution optimisation with respect to memory size (including the choice of a proper structure). No auxiliary logical elements can be used except those which result directly from the selected structure of a mircoprogrammable circuit.



Gray counter

Q_1^n	Q_0^n	Q_1^{n+1}	Q_0^{n+1}	a_1	a_0	Z_2	Z_1	Z_0
a	b	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0
0	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	0
1	1	0	1	1	1	1	1	0
1	0	1	0	1	0	1	0	1