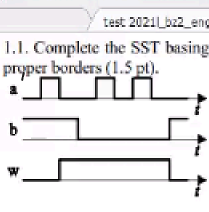
1.1. Complete the SST basing on time diagram. If the table is not solvable, mark the placement of the proper borders (1.5 pt).



Cycle	1	2	3	4	5	6	7	8	9	10
a	–	+	–			+	–	+	–	
b	+				–					+
w	–		+							
NCS	2_2	3	2_1	6	4	5	4	5	4	6_1

1.2. For the SST given below provide:

Cycle	0	1	2	3	4	5	6	7	8	9	10	11	12	13	0
2^0 x_1	+				-	+	-				+	-		+	
2^1 x_2	-	+		-				+	-	+					-
2^2 z	+		-										+		
NCS	5	7_0	3_0	1_0	0_0	1_0	0_0	2_0	0_0	2_0	3_0	2_1	6	7_1	5

I III +
II IV –

a) the solvable table (1 pt),

Cycle	0	0'	1	2	2'	3	4	4'	5	6	7	8	9	10	10'	11	12	13	0
2^0 x_1	+						-		+	-				+		-		+	
2^1 x_2	-		+			-					+	-	+						-
2^2 z	+			-													+		
2^3 q		+				-			+						-				
NCS	5_1	13_1	15_1	11_1	3_1	1_1	0_1	8_1	9	8_1	10_1	9	10_1	11	3_1	2_1	6_1	7_1	5

b) definitions of functions describing the circuit in the canonical form (0.5 pt).

$Z = \begin{cases} \Sigma(2,5,6,7,13)_{qzx_2x_1} \\ \Pi(0,1,3,8,9,10,11,15)_{qzx_2x_1} \end{cases}$ $\quad Q = \begin{cases} \Sigma(0,5,8,9,10)_{qzx_2x_1} \\ \Pi(1,2,3,6,7,11)_{qzx_2x_1} \end{cases}$

1.3. For the function definitions given below, provide the minimal expressions for implementation: a) for Z using NOR gates (1 pt), b) for W using $\sim sr$ flip-flop (1 pt).

$Z = \begin{cases} \sum(3,5,6,7,14,15)_{zwba} \\ \prod(0,1,2,4,8,9,10,11)_{zwba} \end{cases}$ $\quad W = \begin{cases} \sum(1,6,9,10,11,14)_{zwba} \\ \prod(0,2,3,4,5,7,8,15)_{zwba} \end{cases}$

zw \ ba	00	01	11	10
00	0	0	1	0
01	0	1	1	1
11	–	–	1	1
10	0	0	0	0

Z

zw \ ba	00	01	11	10
00	0	1	0	0
01	0	0	0	1
11			0	1
10	0	1	1	1

W

zw \ ba	00	01	11	10
00	0	1	0	0
01	0	0	0	1
11			0	1
10	0	1	1	1

W

$Z = wb + \bar{z}wa + \bar{z}ba$

$\sim s_W = w + b + \bar{a}$

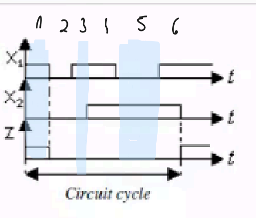
$r_W = \bar{b}\bar{a} + wa$

1. Sequence Switching Table method

$s_w = \bar{w}\bar{b}a$

$\bar{s}_w = w + b + \bar{a}$

2.1. For the circuit described by the timing chart provide the primitive flow map (1.0 pts).



s^n \ x_1x_2	00	01	11	10	Z
1)	2			(1)	1
2)	(2)			3	0
3)			4	(3)	0
4)		5	(4)		0
5)		(5)	6		0
6)			(6)	1	0

	ab 00	01	11	10	W
0	7		1	(0)	0
1		2	(1)	4	1
2		(2)	1		1
3	~~[illegible]~~				
4	7		1	(4)	1
5	~~[illegible]~~				
6	~~[illegible]~~				
7	(7)			0	1
8	~~[illegible]~~				
9	~~[illegible]~~				

2.2. For the primitive flow map given, list equivalent and pseudo-equivalent states, and conduct the 1st reduction stage (1.5 pts).

1 - 3 - 5
0 - 8 → 7 - 9
4 - 6

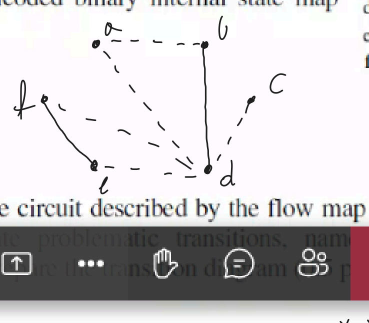
	00	01	11	10	W
0,8	7		1	(0)	0
1,3,5		2	(1)	4	1
4,6	7		1	(4)	1
2		(2)	1		1
7,9	(7)			0	1

2. Huffman's method

2.3. For the flow table given conduct the reduction of compatible states (2nd reduction stage) for Mealy machine, obtaining the minimal number of rows. Draw the merger diagram (0.5 pts), present the symbolic flow map, encoded binary internal state map (eliminate possible races), and output map (1.0 pts).

	x_1x_2 00	01	11	10	W
a	2		1	(0)	1
b		3	(1)	0	0
c	(2)			4	1
d		(3)	1		0
e	5		1	(4)	1
f	(5)			4	1

e, f
a, b, d
c



non critical race

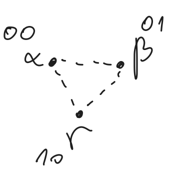
$q_1 q_2$ \ $x_1 x_2$	00	01	11	10
a 00	00	01		10
b 01	01	01	10	11
c 11	00	01	11	11
d 10	10	01	10	10

critical race

critical race

2.4. Analyse the circuit described by the flow map with respect to races ... ing races ...

39:32



α a, b, d
β c
γ e, f

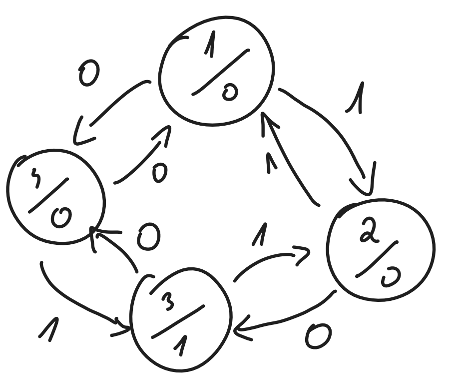
	x_1x_2 00	01	11	10
α	2	(3)	(1)	(0)
β	(2)			4
γ	(5)		1	(4)

x_1x_2	00	01	11	10
00	01/1	00/0	00/0	00/1
01	01/1			11/1
11				10/1
10	10/1		00/1	10/1

3.1. Design the graph for the sequential circuit detecting that the sum of bits in 2-bit words given to the serial input X equals to 1. It should be signalled by setting the output W=1 for the single clock period (1.5 pt).

w=1 dla: ? zależy czy normalnie czy binarnie

10 / 01 / 11



3.2. Design the parallel counter with a programming input p and counting codes as given below. Apply synchronous illegal state recovery. Provide the binary program map (2 pt).

p=0 | 11→10→00

p=1 | 01→10→11

p=0 3 → 2 → 0

p=1 1 → 2 → 3

s^n \ p	0	1
0	3	1
1	3	2
2	0	3
3	2	1

$Q_1^nQ_0^n$ \ p	0	1	W
00	11	01	00
01	11	10	01
11	10	01	11
10	00	11	10

$Q_1^{n+1}Q_0^{n+1}$

3.3. For the circuit described by the program map present the equations for the implementation for T flip-flops (1.5 pt).

$Q_1^nQ_0^n$ \ p	0	1
00	10	00
01	11	10
11	11	01
10	11	00

Q_1^{n+1} Q_0^{n+1}

$Q_1^nQ_0^n$ \ p	0	1
00	1	0
01	1	1
11	0	1
10	0	1

T_1

$Q_1^nQ_0^n$ \ p	0	1
00	0	0
01	0	1
11	0	0
10	1	0

T_0

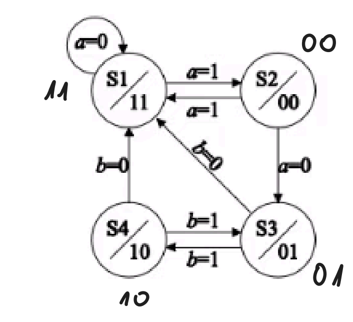
$T_1 = \bar{Q}_1\bar{p} + \bar{Q}_1Q_0 + Q_1p$

$T_0 = \bar{Q}_1Q_0p + Q_1\bar{Q}_0\bar{p}$

4. Design microprogrammable circuit working according to the presented graph. The solution should be as optimal as possible in respect to the memory size. Provide the solution in the form of:

a) microprogram proper for the given diagram (2.5 pt),

	Q_1^n A_1	Q_0^n A_0	Q_1^{n+1} y_5	Q_0^{n+1} y_4	a_1 y_3	a_0 y_2	Z_1 y_1	Z_0 y_0
S_2	0	0	1	1	0	0	0	0
S_3	0	1	1	1	0	1	0	1
S_4	1	0	0	1	1	0	1	0
S_1	1	1	1	1	1	1	1	1

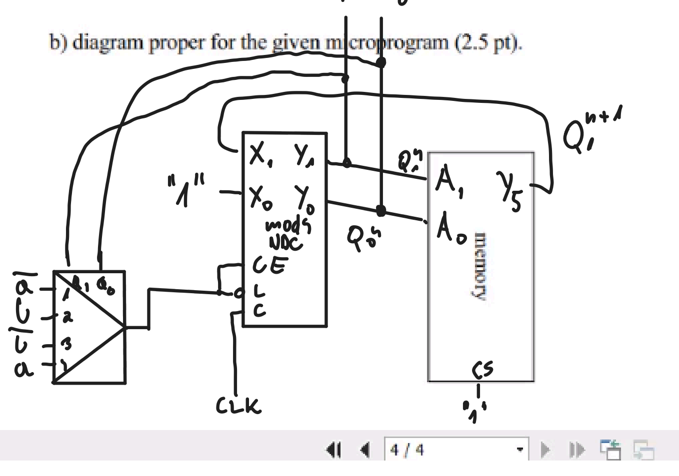


$Q_1^n = a_1 = Z_1$

$Q_0^n = a_0 = Z_0$

$Q_0^{n+1} = 1$

b) diagram proper for the given microprogram (2.5 pt).



4. Microprogrammable circuits