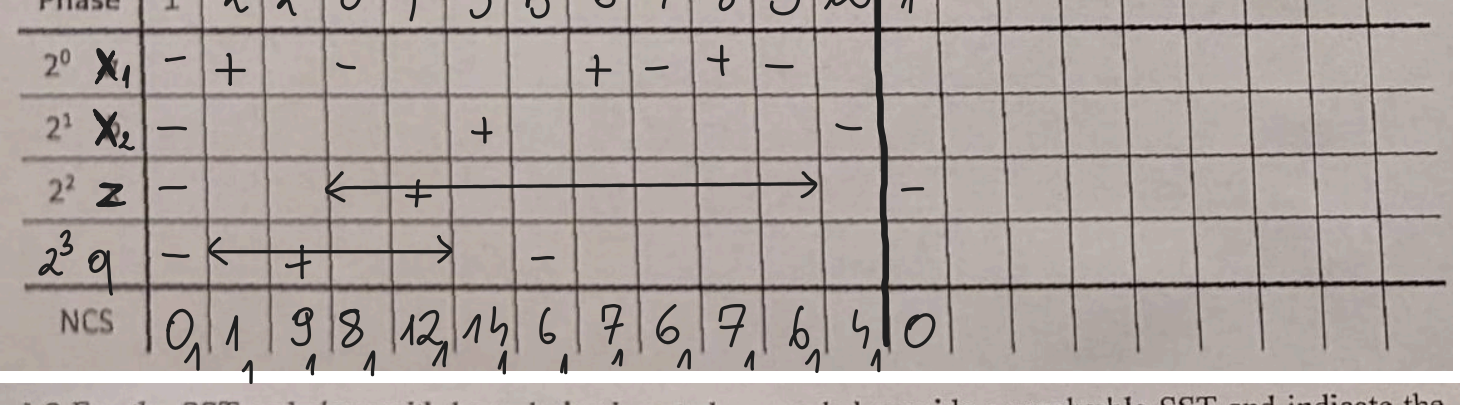
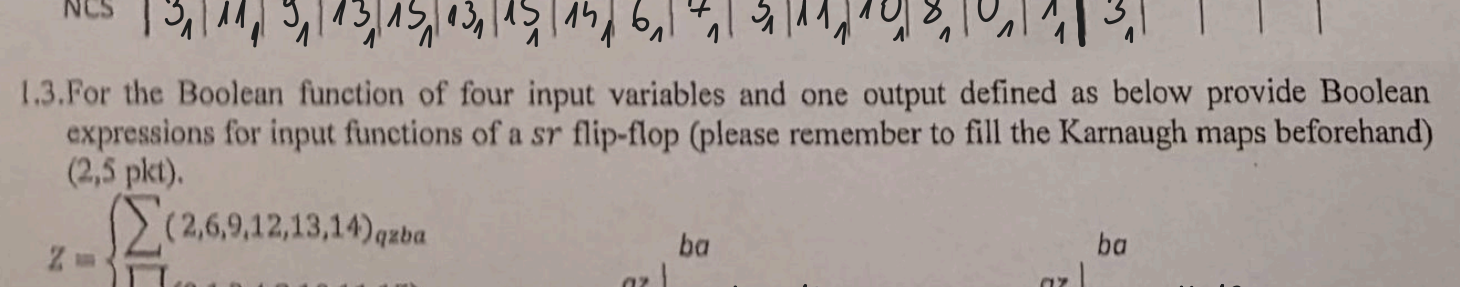




Phase	1	2	3	4	5	6	7	8	9	10	11	12	1
2^0 a	+						-	+		-		+	
2^1 b	+	-		+	-	+					-		+

$2_0, 0_0$
 $1_1, 5_1, 7_1, 6_1$

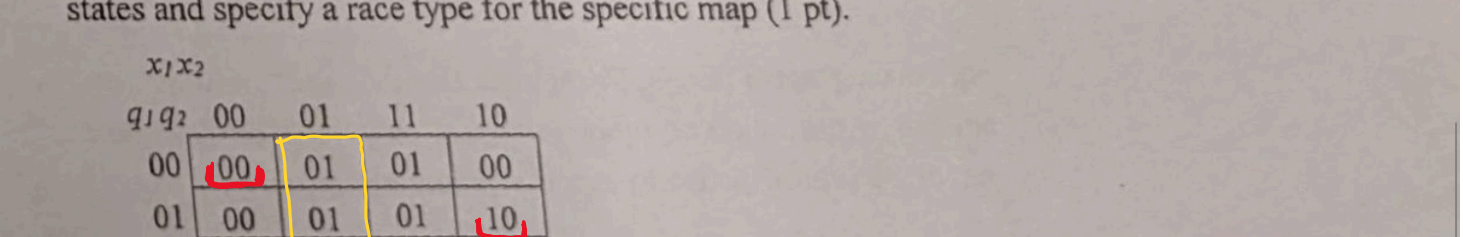
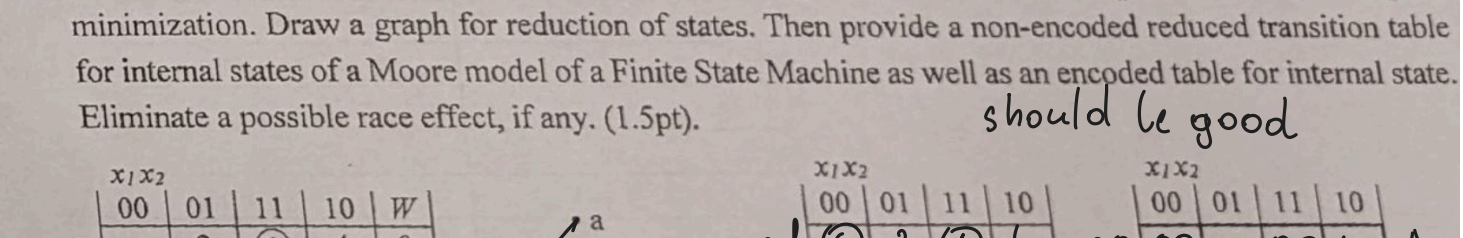


$$\begin{array}{c} 01 \\ 11 \\ 10 \end{array} \begin{array}{ccc} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 0 \end{array} \begin{array}{c} 1 \\ 1 \\ 0 \end{array} \quad \begin{array}{c} 01 \\ 11 \\ 10 \end{array} \begin{array}{ccc} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 0 & 1 & 0 \end{array} \begin{array}{c} 1 \\ 1 \\ 0 \end{array}$$

2.1 For an asynchronous sequential circuit defined by the graph below provide a primary transition table for the control routine. (1 pt).

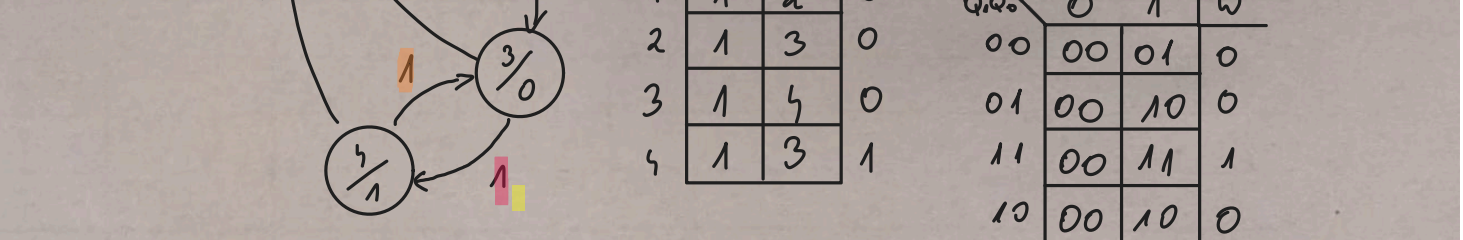
	ab					
	00	01	11	10	XY	
1)	①	2			0	
2)	1	② 3			0	

5)

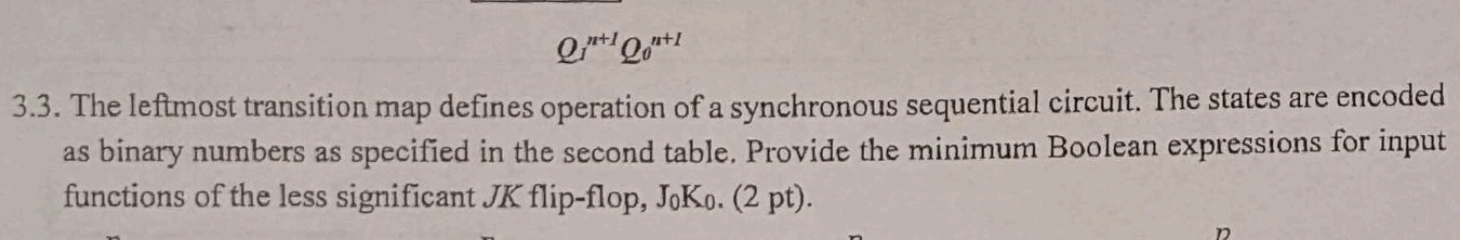


10 10 01 10 10 00

critical race non critical race 2/4



3.2. Design a programmable parallel counter with the programming input of p . The counter should count input signals according to the sequence as below. The internal state of the circuit must correspond to the counter content expressed in the natural binary code. Provide synchronous correction to the initial state of 00q1q0. Fill the non-encoded and encoded transition map (1.5 pt).



0	1	2	00	01	10	00	11	00	-	-	00	-	-
1	3	0	01	11	00	01	-	-	01	0	1	01	1
2	0	3	11	00	11	11	-	-	11	1	0	10	0
			10			10			10				

