

### Silesian University of Technology



# Department of Graphics, Computer Vision and Digital Systems

Year	Type*: SSI/NSI/NSM	Subject: Assembler Programming Languages	Group	Section
2024/2025	SSI	APL – LAB	1	1
Tutor:	dr inż. Adam Opara		Class date: ( week day, hour)	
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Contact Email:	1	8.30 – 10.00		
Report				



### Task 1

Create procedure CheckSSECpp returning 1 if procesor supports SSE.

```
extern "C" int CheckSSECpp() {
   int cpuInfo[4];
   __cpuid(cpuInfo, 1);
   return (cpuInfo[3] & (1 << 25)) ? 1 : 0;
}</pre>
```

CheckSSECpp uses the C++ intrinsic \_\_cpuid() to check if the processor supports SSE (Streaming SIMD Extensions). When \_\_cpuid is called with EAX=1, bit 25 of EDX in the returned cpuInfo array indicates whether SSE is available. The function returns 1 if SSE is supported, otherwise 0.

### Task 2

Create an assembly DLL with a procedure CheckSSEAsm checking availability of SSE instructions, and with RadToDegAsm function.

```
.code
PUBLIC CheckSSEAsm
PUBLIC RadToDegAsm

CheckSSEAsm PROC
    mov eax, 1
    cpuid
    bt edx, 25 ; check SSE bit (bit 25 in EDX)
    setc al ; set AL = 1 if bit was set
    movzx eax, al ; zero-extend to full EAX
    ret
CheckSSEAsm ENDP
```

CheckSSEAsm is a pure x64 assembly implementation that uses the cpuid instruction to query processor features. It sets EAX to 1 and executes cpuid, then checks bit 25 of EDX using bt. If the bit is set (SSE supported), the result is 1, otherwise 0.

```
RadToDegAsm PROC
    movsd xmm1, qword ptr [dbl180]
    movsd xmm2, qword ptr [dblPI]
    divsd xmm1, xmm2
    mulsd xmm0, xmm1
    movsd qword ptr [tempDeg], xmm0
    cvttsd2si rax, xmm0
    cvtsi2sd xmm3, rax
    subsd xmm0, xmm3
    movsd xmm4, qword ptr [db160]
    mulsd xmm0, xmm4
    imul rax, 100
    cvtsi2sd xmm3, rax
    addsd xmm0, xmm3
    ret
RadToDegAsm ENDP
.data
dblPI REAL8 3.141592653589793
dbl180 REAL8 180.0
db160 REAL8 60.0
tempDeg REAL8 0.0
END
```

RadToDegAsm is a SIMD-based function written in x64 assembly using SSE2 (xmm registers). It converts an angle in radians to the NMEA coordinate format (DDDMM.mmmm), used in GPS.

#### Procedure:

- multiplies the input radians by  $\frac{180}{\pi}$  to get degrees
- · splits degrees into integer and fractional parts
- · converts the fractional part to minutes
- returns the final result as | intDeg | imes 100 + | minutes |

All calculations use floating-point SIMD registers (xmm0 - xmm4).

### Task 3

Create procedure RadToDegCpp in C++ .

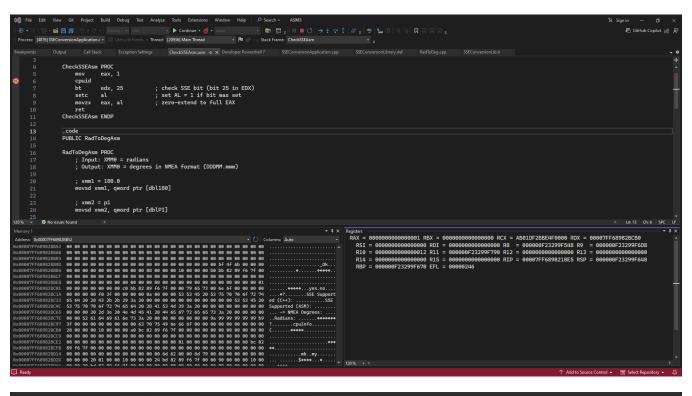
```
extern "C" double RadToDegCpp(double radians, int sseEnabled) {
   double dDeg = 0.0;
   if (sseEnabled) {
        __m128d ma, mb, mDeg, mx, my, mz, mk;
        ma = _mm_set_sd(180.0);
        mb = _mm_set_sd(3.141592653589793);
        mDeg = _mm_div_pd(ma, mb);
        ma = _mm_set_sd(radians);
        mb = _mm_mul_pd(ma, mDeg);
        dDeg = mb.m128d f64[0];
        int nDeg = (int)dDeg;
        double dRem = dDeg - nDeg;
        ma = _mm_set_sd(100.0);
        mb = _mm_set_sd(60.0);
        mx = mm set sd(dRem);
        mz = _mm_mul_pd(mx, mb);
        mk = _mm_set_sd(nDeg * 100.0);
        my = _mm_add_pd(mk, mz);
        return my.m128d_f64[0];
   } else {
        double dDeg = radians * 180.0 / 3.141592653589793;
        int nDeg = (int)dDeg;
        double dRem = dDeg - nDeg;
        return nDeg * 100.0 + dRem * 60.0;
   }
}
```

RadToDegCpp performs the same conversion from radians to NMEA degrees format as the assembly version, but in C++ . It supports two modes:

- SSE2 mode: uses \_mm\_set\_sd , \_mm\_div\_pd , \_mm\_mul\_pd , and other intrinsics to perform vectorized floating-point math.
- Fallback mode: if SSE is not available, the calculation is done using standard scalar operations.

### Task 4

Compile and run an application that calls procedures CheckSSExxx and RadToDegxxx.



## **Conclusions**

In this lab, I learned how to detect SSE support using both C++ and x64 Assembly. The SSE detection worked correctly in both languages, and the conversion produced accurate results. Writing SIMD code in Assembly was more complex, but it gave better control over registers. This lab helped me understand how modern CPUs handle floating-point operations efficiently.